Carrier pocket engineering to design superior thermoelectric materials using superlattice structures

The concept of Carrier Pocket Engineering is applied to GaAs/AlAs and Si/Ge superlattices to obtain a large thermoelectric figure of merit $Z_{3D}/T$. For both GaAs/AlAs and Si/Ge systems, the calculated values for $Z_{3D}/T$ (0.4 and 0.96 for GaAs/AlAs and Si/Ge superlattices, respectively, at 300 K) are greatly enhanced relative to those for the corresponding bulk materials. We propose that the key to obtain such enhancements in $Z_{3D}/T$ is the careful optimization process of the structure and geometries of the superlattice, so that we can make use of the higher energy valleys in the 3D conduction band, that have no effect on electron transport in the bulk semiconductor, but can contribute to the thermoelectric transport in the superlattice form. Other advantages of having superlattice structures, such as the increased scattering of phonons to reduce the lattice conductivity and the lattice strain effect in Si/Ge superlattices to control the conduction band offset, are also discussed.